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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,983	ZOMMER ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The finality of the rejection of the last Office action is withdrawn in view of the new ground of rejection.

2. Claim 7 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 1, the parent claim of claim 7, discloses a combined current density of said active cells fabricated according to said second cell design is greater than a combined current density of said active cells fabricated according to said first cell design during operation of said active cells. Claim 7 only discloses said first cell design differs from said second cell design with respect to current density. Therefore, claim 7 is not further limit the subject matter of claim 1.

3. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses a plurality of terminating cells about a periphery of said active region as claimed in claim 15.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 7, 9, 10, 12 and 14 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Dupuy et al.

In regards to claim 1, Dupuy et al. inherently teach a method for manufacturing a semiconductor power device in figs. 10 and 11. It comprising: identifying an active region on a semiconductor die [35], the active region having a central portion [121] and a first peripheral portion [122-125] disposed about a periphery of said central portion; identifying a first region [121] in said central portion of said active region; identifying a second region [122-125] in said first peripheral portion of said active region; fabricating active cells [111] in accordance with a first cell design (the transistors [111] are fabricated with short distance [117] between the source regions [114]) in said first region; fabricating active cells in accordance with a second cell design (the transistors [112] are fabricated with long distance [116] between the source regions [114]) in said second region, wherein a combined current density of said active cells fabricated according to said second cell design is greater than a combined current density of said active cells fabricated according to said first cell design during operation of said active cells (col. 6, lines 44-47, col. 6, line 65 to col. 7, line 15).

In regards to claim 2, Dupuy et al. further disclose said first cell design and said second cell design include cell dimensions such that a cell density of said first region is different from that of said second region (there are more transistors [112] in the second region [122-125] than the first region [121]).

In regards to claim 3, Dupuy et al. further disclose said first cell design includes at least one physical dimension (the distance between the source regions [114]) different from that included in said second cell design.

In regards to claim 7, Dupuy et al. further disclose said first cell design differs from said second cell design with respect to current density (col. 6, line 65 to col. 7, line 15).

In regards to claim 9, Dupuy et al. inherently disclose said first cell design differs from said second cell design with respect to transconductance because the current density of the first cells is different than that of the second cells.

In regards to claim 10, Dupuy et al. inherently disclose said first cell design differs from said second cell design with respect to gain because the current density of the first cells is different than that of the second cells.

In regards to claim 12, Dupuy et al. disclose said first cell design and said second cell design are field effect transistors.

In regards to claim 14, Dupuy et al. further disclose a semiconductor power device fabricated in accordance with the method of claim 1.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3-5, 8, 15 and 16 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ito et al.

In regards to claim 1, Ito et al. inherently teach a method for manufacturing a semiconductor power device in figs. 1 and 4. It comprising: identifying an active region (a region on the upper right hand corner of fig. 4 that includes 4 first source cells [120], 4 second source cells [121] and 2 drain cells [122]) on a semiconductor die [101], the active region having a central portion (a region with 2 first source cells [120] adjacent to 4 second source cells [121]) and a first peripheral portion (a region with 6 second source cells [121], 2 drain cells [122] and 2 first source cells [120]) disposed about a periphery of said central portion; identifying a first region (a region with 2 first source cells [120] adjacent to 4 second source cells [121]) in said central portion of said active region; identifying a second region (a region with the 6 second source cells [121], 2 drain cells [122] and 2 first source cells [120]) in said first peripheral portion of said active region; fabricating active cells [120] in accordance with a first cell design (the source cells [120] are fabricated with a square shape) in said first region; fabricating active cells in accordance with a second cell design (the source cells [121] with a rectangular shape) in said second region, wherein a combined current density of said active cells fabricated according to said second cell design is greater than a combined current density of said active cells fabricated according to said first cell design during operation of said active cells (Since the second source cells [121] have longer channel width than the first source cells [120], the second source cells can conduct more current than the first source cells).

In regards to claim 3, Ito et al. further disclose said first cell design includes at least one physical dimension (the size of the source cell) different from that included in said second cell design.

In regards to claim 4, Ito et al. further disclose said physical dimension includes a channel width (the size of the source cell determines the channel width).

In regards to claim 5, Ito et al. further disclose said physical dimension includes a cell die area (the size of the first source cell [120] different from the size of the second source cell [121]).

In regards to claim 8, Ito et al. further disclose said first cell design differs from said second cell design with respect to source resistance. (Since the size of the first source cell is different than that of the second source cell, the size of the source region in the first source cell is different than that of the source region in the second source cell. The source resistance in the first source cell is different than the source resistance in the second source cell.)

In regards to claim 15, Ito et al. further disclose a plurality of terminating cells (the rest of the cells [120, 121] other than the cells [120, 121] in the upper right hand corner of fig. 4) about a periphery of said active region.

In regards to claim 16, Ito et al. further disclose said active region further has a second peripheral portion (a region where the rest of the cells [120, 121] are formed) disposed about a peripheral region of said first peripheral portion, the method further comprising identifying a third region (the region where the rest of the cells [120, 121] are formed) in said second peripheral portion and fabricating active cells [120, 121] in

accordance with a third cell design (the shapes of the first and second source cells [120, 121]) in said third region, wherein during operation of said active cells a combined current density of said active cells fabricated according to said third cell design is greater than both said combined current density of said active cells fabricated according to said first cell design and said combined current density of said active cells fabricated according to said second cell design. (Since there are more source cells [120, 121] in the third region than in the first and second regions, a combined current density of said active cells fabricated according to said third cell design is greater than both said combined current density of said active cells fabricated according to said first cell design and said combined current density of said active cells fabricated according to said second cell design.).

8. Claims 1, 6, 11, 13 and 17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Colwell et al.

In regards to claim 1, Colwell et al. inherently teach a method for manufacturing a semiconductor power device in fig. 2b. It comprising: identifying an active region [150] on a semiconductor die, the active region having a central portion and a first peripheral portion (a portion on the right side of the central portion in fig. 2b) disposed about a periphery of said central portion; identifying a first region in said central portion of said active region; identifying a second region in said first peripheral portion of said active region; fabricating active cells [154] in accordance with a first cell design (the transistors [154] are fabricated with short gate widths) in said first region; fabricating active cells [152] in accordance with a second cell design by (the transistors [152] are fabricated

with long gate widths) in said second region, wherein a combined current density of said active cells fabricated according to said second cell design is greater than a combined current density of said active cells fabricated according to said first cell design during operation of said active cells (The transistors with the longer gate widths conduct more current than the transistors with the shorter gate widths.).

In regards to claim 6, Colwell et al. further disclose the first cell design includes a material composition (n-type dopants in source and drain regions) for cells that is different from that of said second cell design (p-type dopants in source and drain regions).

In regards to claim 11, Colwell et al. further disclose said first cell design differs from said second cell design with respect to threshold voltage (the NMOS transistors [154] have a different threshold voltage than the PMOS transistors [152]).

In regards to claim 13, Colwell et al. further disclose said first cell design and said second cell design are memory cells (col. 1, lines 37-42, (Colwell et al. disclose a gate array.)).

In regards to claim 17, Colwell et al. inherently show a method for manufacturing a semiconductor power device in fig. 2b. It comprising: identifying an active region on a semiconductor die; identifying a first region (a region occupied by a first group of transistors [154]) in said active region; identifying a second region (a region occupied by a second group of transistors [171]) in said active region; identifying a third region (a region occupied by a third group of transistors [152]) in said active regions; providing a first cell design by which active cells in said first region will be fabricated; and providing

a second cell design by which active cells in said second region will be fabricated; and providing a third cell design by which active cells in said third region will be fabricated, wherein first active cells (NMOS) fabricated according to said first cell design are different from second active cells (NMOS) fabricated according to said second cell design, wherein third active cells (PMOS) fabricated according to said third cell design are different from said first active cells and from said second active cells, wherein said first cell design and said second cell design are memory cells (col. 1, lines 37-42, (Colwell et al. disclose a gate array.)).

9. Applicant's arguments filed 9/26/05 have been fully considered but they are not persuasive.

It is urged, in page 6 of the remarks, that Colwell et al. do not show or suggest active cells fabricated in accordance with a first cell design in a central portion of an active region and active cells fabricated in accordance with a second cell design in a first peripheral portion, where the combined current density of the second active cells is greater than the combined current density of the first active cells. However, Colwell et al. show active cells [154] fabricated in accordance with a first cell design in a central portion of an active region and active cells [152] fabricated in accordance with a second cell design in a first peripheral portion. Since the gate widths of the second active cells [152] are larger than the gate widths of the first active cells [154], the combined current density of the second active cells [152] is greater than the combined current density of the first active cells [154].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
October 6, 2005

Steven Loke